Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1-11 (cancelled).

12 (original): A noise-proof clock signal circuit capable of diminishing noises in a clock signal transmitted over a bus, the circuit comprising:

a conduction line module comprising the bus and at least a conduction line disposed along the bus, the bus having a first end for inputting the clock signal, and each of the conduction lines having a first end connected to a reference voltage;

a voltage averaging circuit having input ends connected to second ends of the conduction lines for generating an arithmetic mean voltage of voltages at the second ends of the conduction line and an output end for outputting the arithmetic mean voltage; and

a voltage detection circuit electrically connected to a second end of the bus and the output end of the voltage averaging circuit for generating an amended clock signal by determining a voltage difference between the arithmetic mean voltage and a voltage at the second end of the bus.

13 (original): The circuit of claim 12 wherein each of the conduction lines is disposed in parallel with the bus.

14 (original): The circuit of claim 12 wherein the conduction lines comprise two conduction lines respectively disposed on two opposite sides of the bus.

15-18 (cancelled).

19 (original): A method for diminishing noises in a clock signal transmitted over a bus, the method comprising:

inputting the clock signal to an input end of the bus;

providing at least a conduction line disposed along the bus, each of the conduction lines having an input end connected to a reference voltage;

calculating an arithmetic mean voltage of voltages at output ends of the conduction lines; and

outputting an amended voltage by determining a voltage difference between the arithmetic mean voltage and a voltage at an output end of the bus.

20 (original): The method of claim 19 wherein the conduction lines all are disposed in parallel with the bus.

21 (currently amended): The method of claim 19 wherein the conduction lines ~~of the conduction line module~~ comprise two conduction lines respectively disposed on two opposite sides of the bus.

22 (new): The circuit of claim 12 wherein the reference voltage is generated from a reference circuit.

23 (new): The circuit of claim 22 wherein the reference circuit comprises a first resistor and a second resistor connected in series with the first resistor, the first resistor having a first end connected to a first voltage and a second end connected to the first end of the conduction line, and the second resistor having a first end connected to a second voltage and a second end connected to the first end of the conduction line.

24 (new): The circuit of claim 12 wherein the voltage detection circuit comprises an operational amplifier.

25 (new): The circuit of claim 12 wherein the clock signal is generated from a bus master.

26 (new): The circuit of claim 25 wherein the bus master is a south bridge circuit.

27 (new): The circuit of claim 25 wherein the bus master is a keyboard controller.

28 (new): The circuit of claim 12 wherein the amended clock signal is transmitted to a bus slave.

29 (new): The circuit of claim 28 wherein the bus slave is a memory module.

30 (new): The circuit of claim 12 wherein the bus is a smart bus (SMBUS).

31 (new): The circuit of claim 28 wherein the bus slave is a clock generator.

32 (new): The circuit of claim 28 wherein the bus slave is a peripheral device.

33 (new): The method of claim 19 wherein the bus is a SMBUS.

34 (new): The method of claim 19 wherein the clock signal is generated from a bus master and the amended clock signal is transmitted to a bus slave.